REMARKS/ARGUMENTS

The present Amendment is responsive to the non-final Office Action mailed September 3, 2008 in the above-identified application.

Claims 1-20 are amended to clarify features recited thereby. These amendments are fully supported by applicant's disclosure, see, for example, Specification, page 16, lines 6-13 (and refer to Figs. 3-5) and Specification, page 18, line 20 – page 19, line 2 (and refer to Fig. 6) of the published international application with respect to the amendments to claim 1 regarding the block queue feature and the modification of the memory address mapping table in accordance therewith.

Applicant thanks the Examiner for acknowledging review and consideration of the references cited in the Information Disclosure Statements filed on July 19, 2006 and February 19, 2008.

Rejection of Claim 5 under 35 U.S.C. § 112, Second Paragraph

Claim 5 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite on the ground that the recitation "the control data storage sector" lacks sufficient antecedent basis. Claim 5 is amended.

Rejection of Claims 1-15 under 35 U.S.C. § 103

Claims 1-15 are rejected under 35 U.S.C. § 103 as being obvious from Ban, U.S. Patent No. 5,404,485 in view of Higuchi et al., U.S. Patent Application Publication No. 2002/0120820. Reconsideration of this rejection is respectfully requested.

Without intending to limit the scope of the claims, an advantage or effect according to an aspect of applicant's invention as claimed in claim 1 is that an available physical address region can be located rapidly because the master control unit refers to the head of a block queue that lists an available physical address region in the physical memory space. As recited in claim 1, a block queue listing the physical address regions is provided so that the logical address can be conveniently and speedily associated with a new physical address region for writing the data received.

Claim 1 requires a portable data storage device including a master control unit operable to to determine whether the physical address corresponding, according to the memory address

mapping table, to the logical address is in an erased state, and when the result of this determination is negative, to modify the memory address mapping table in accordance with a block queue listing one or more queuing physical address regions to thereby associate a second physical address region with the logical address region containing the logical address, the second physical address region being a queuing physical address region at a head of the block queue. Further, claim 1 requires that the master control unit then writes the data to the second physical address region.

Ban discloses a flash memory and virtual mapping system that allows data to be continuously written to unwritten physical address locations using a virtual memory map that relates flash memory physical location addresses for tracking the location of data in the flash memory (Ban, Abstract). Ban discloses that, in a write operation, if a block corresponding to a virtual address has been written in, a controller of the flash memory scans a block allocation map to locate a free block within a unit of that flash memory. The status of the written block and the status of the free block are then updated accordingly (Ban, column 5, line 36 – column 6, line 2; Fig. 6).

Ban is silent with respect to any block queue that lists one or more queuing physical address regions, as required by claim 1. As discussed, Ban discloses that the flash memory is scanned to locate a free block when needed.

The Office Action, paragraph 7 appears to be in error when it states that the feature of "queuing physical memory regions" previously recited in claim 6 is disclosed by Ban, Figs. 3 and 4. Ban, Fig. 3 illustrates a flash memory unit having a unit header, a block allocation map and data blocks within the memory unit. Fig. 4 of Ban illustrates the mapping of virtual addresses to physical addresses in the flash memory. Ban, Figs. 3 and 4 do not disclose or suggest any kind of queue that lists physical memory regions. Accordingly, Ban does not disclose or suggest the recitations of claim 1.

Moreover, it is respectfully submitted that the recitations of claim 1 would not have been obvious from Ban for the following additional reason. The block allocation map disclosed by Ban is a mapping between respective block numbers and logical block addresses at respective rows. Thus, Ban discloses a scanning algorithm that sequentially inspects the rows of the block allocation map to locate the free block. Thus, Ban actually teaches away from a block queue because Ban is directed to sequential inspection of the rows, rather than to a non-sequential

inspection of the head of the block queue to locate an available physical address region. As discussed, such scanning of the block allocation map to locate the free block, as discussed by Ban, necessarily entails time that must be expended to inspect sequentially the rows of the block allocation map. Therefore, the recitations of claim 1 would not have been obvious from Ban.

Higuchi discloses a memory device that includes nonvolatile memory, a volatile memory that may be random-accessed and a controller that transfers data between the nonvolatile memory and the volatile memory and enables a pseudo access as if the volatile memory were externally directly accessed in accordance with an instruction through an external bus when data transfer is not performed (Higuchi, Abstract).

Higuchi is silent with respect to any block queue listing one or more queuing physical address regions, as required by claim 1. Higuchi discloses that an access to a NOR flash memory is allowed even during data transfer between a NAND flash memory and the RAM. Accordingly, even taken together in combination, Higuchi and Ban do not disclose or suggest the recitations of claim 1.

Claims 2-15 depend from claim 1 and are therefore patentably distinguishable over the cited art for at least the same reasons.

Rejection of Claims 17-20 under 35 U.S.C. § 103

Claims 17-20 are rejected under 35 U.S.C. § 103 as being obvious from Ban and Higuchi in view of Horn et al., U.S. Patent Application Publication No. 2005/0050273. Reconsideration of these rejections is respectfully requested.

Horn discloses a networked storage system, including a RAID (Redundant Arrays of Independent Disks) controller for use in networked storage systems.

Horn is unconcerned with a portable data storage device as claimed in claim 1, and does not even remotely disclose or suggest a portable data storage device including a master control unit that refers to a block queue listing one or more physical address regions, as further required by claim 1. Further, the Office Action does not allege that Horn discloses or suggests such features. Therefore, even taken together in combination, Horn, Higuchi and Ban do not disclose or suggest the recitations of claim 1.

Claims 17-20 depend from claim 1 and are therefore patentably distinguishable over the cited art for at least the same reasons.

In view of the foregoing, withdrawal of the rejections and allowance of the claims of the application are respectfully requested.

Respectfully submitted,

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